APPLICATION DATA SHEET

APPLICATION INFORMATION

Filing Date::	03-09-2004
Application Type::	Regular
Subject Matter::	Utility
Title::	FPGA Configuration Memory with Built-In Error Correction Mechanism
Attorney Docket Number::	X-812-1P US
Request for Early Pub?::	No
Request for Non-Pub?::	Yes
Total Drawing Sheets::	13
Small Entity?::	No
Petition included?::	No

APPLICANT INFORMATION

Applicant Authority Type::	Inventor
Primary Citizenship Ctry::	US
Status::	Full Capacity
Given Name::	Stephen
Middle Name::	M.
Family Name::	Trimberger
Street::	1261 Chateau Drive
City::	San Jose
State or Province::	California
Postal or Zip Code::	95120

Applicant Authority Type::	Inventor
Primary Citizenship Ctry::	US
Status::	Full Capacity
Given Name::	Austin
Middle Name::	H.
Family Name::	Lesea
Street::	25542 Mt. Bache Road
City::	Los Gatos

State or Province:: California
Postal or Zip Code:: 95033

Applicant Authority Type:: Inventor
Primary Citizenship Ctry:: US
Status:: Full Capacity
Given Name:: Derek
Middle Name:: R.
Family Name:: Curd
Street:: 6505 Hirabayashi Drive
City:: San Jose
State or Province:: California
Postal or Zip Code:: 95120

CORRESPONDENCE INFORMATION

Correspondence Customer Number:: 24309

REPRESENTATIVE INFORMATION

Representative Customer Number::	**24309**	

DOMESTIC PRIORITY INFORMATION

Application::	**Continuity Type::**	**Parent Application::**	**Parent Filing Date::**
This Applic.	CIP	09/797,138	02-28-01

ASSIGNEE INFORMATION

Assignee Name:: Xilinx, Inc.
Street:: 2100 Logic Drive
City:: San Jose
State or Province:: California
Postal or Zip Code:: 95124